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JAMES H. BEUSSE, ESQUIRE
BEUSSE BROWNLEE BOWDOIN & WOLTER, P.A.
SUITE 2500
390 NORTH ORANGE AVENUE
ORLANDO, FL 32801

EXAMINER	
PERALTA, GINETTE	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/026,257	Applicant(s) HUANG ET AL.	
	Examiner Ginette Peralta	Art Unit 2814	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1 and 2 are rejected under 35 U.S.C. 102(e) as being anticipated by Fornof et al. (U. S. Pat. 6,537,908 B2).

Regarding claim 1, Fornof et al. discloses in figs. 2A to 2F a method of forming an interconnect structure of a semiconductor device, the interconnect structure having a dielectric material 52 deposited over an underlying interconnect layer 50 and having a via 64 extending through the dielectric material for establishing a connection between an underlying conductor and a trench in an upper portion of the dielectric material, that comprises the steps of forming a mask layer 58/56 over the dielectric material 52; etching the mask layer to a predetermined depth forming a via 60 in the mask layer without exposing the underlying dielectric material (Fig. 2C); then etching the mask layer to a second predetermined depth of the mask layer less than the first predetermined depth forming a trench in the mask layer; forming a via 64 through the

dielectric material 52′ to the underlying conductor 50, corresponding to the dimensions of the via formed in the mask layer; and forming a trench in the dielectric material to a predetermined depth of the dielectric material corresponding to the dimensions of the trench formed in the mask layer.

Regarding claim 2, Fornof et al. discloses a further step of removing a predetermined amount of the mask layer from the semiconductor device and leaving a film of the mask layer thereon over the dielectric material as shown in fig. 2F.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fornof et al. in view of Applicant's admitted prior art (figs. 1 and 2).

Regarding claim 3, Fornof et al. discloses that the dielectric material includes a dielectric layer 52′.

Fornof et al. discloses the claimed invention with the exception of utilizing a multi-layered dielectric layer comprising a via dielectric layer, a trench dielectric layer formed over the via dielectric layer, an etch stop layer disposed between the trench

dielectric layer and the via dielectric layer, and a barrier layer being disposed between the via dielectric layer and the interconnect layer.

Applicant's admitted prior art discloses in figs. 1 and 2, a conventional method of forming an interconnect structure of a semiconductor device, the interconnect structure having a dielectric material deposited over an underlying interconnect layer and having a via extending through the dielectric material for establishing a connection between an underlying conductor and a trench in an upper portion of the dielectric material, wherein the dielectric material includes a via dielectric layer 12 formed over the interconnect layer 11, a barrier layer 14 disposed between the via dielectric layer 12 and the interconnect layer 11, a trench dielectric layer 13 formed over the via dielectric layer 12, and an etch stop layer 15 disposed between the trench dielectric layer 13 and the via dielectric layer 12. Where the multilayer dielectric arrangement and the barrier layer between dielectric layers are used for the purpose of preventing diffusion or migration of impurities (i.e. conductive layer material atoms) into the dielectric layers that could affect the resistance of the dielectric layer or short the circuit, and to enhance the forming of the via and the trench by etching the two dielectric layers instead of a single dielectric layer comprising both structures.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a barrier layer between the via dielectric layer and the interconnect layer and to use a multilayer dielectric layer in the invention of Fornof et al. as the Applicant's admitted prior art teaches that any one of ordinary skill in the art

would use such a layer in order to prevent diffusion or migration of impurities (i.e. conductive layer material atoms) into the dielectric layers that could affect the resistance of the dielectric layer or short the circuit and to improve the formation of the dual damascene structure.

Regarding claim 4, Fornof et al. discloses that etching the via through the dielectric layer and reaching the interconnect layer, and etching the trench through the trench dielectric layer. Fornof et al. as modified by Applicant's admitted prior art, teaches that the etching the via would include etching through the barrier layer in order to expose the interconnect layer as Fornof et al. discloses.

Regarding claim 5, Fornof et al. discloses removing a predetermined amount of the mask layer from the semiconductor device and leaving a film of the mask layer thereon over the dielectric material, as seen in fig. 2F.

5. Claims 6-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fornof et al. in view of Gutsche (WO 01/43171 A1).

Regarding claim 6, Fornof et al. discloses a method of forming an interconnect structure using a mask layer deposited over a dielectric material which has been deposited over an underlying interconnect layer 50, comprising the steps of forming a first mask film 56 over the dielectric material 52 having a known set of properties; forming a second mask film 58 over the first mask film 56 having a known set of etch properties different from the etch properties of the first mask film, and selectively etching the mask films in multiple steps to form the interconnect structure, etching the

mask films to form a via within the mask layer to a first predetermined depth and down to the first mask film without exposing the underlying dielectric layer, and then selectively etching the mask films to form a trench within the mask layer to a second predetermined depth less than the first predetermined depth of the mask layer previously etched in the mask layer.

Thus, Fornof et al. discloses the claimed invention with the exception of forming a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film, and forming a fourth mask film over the third mask film having etch properties substantially identical to the etch properties of the second mask film.

Gutsche discloses a method for fabricating a hard mask on a semiconductor substrate to be applied during contact hole etching or during deep trench etching (¶[0027]) that includes forming a first mask film over the substrate having a known set of etch properties; forming a second mask film over the first mask film having a known set of etch properties different from the etch properties of the first mask film (¶[0022]); forming a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film(¶[0022], [0024]), and forming n mask films over the third mask film having etch properties alternating according to the first and second mask films, for the disclosed intended purpose of providing a hard mask for etching of semiconductor substrates with a high aspect ratio

like vias, the patterning of materials that are difficult to etch or during contact hole etching or trench etching.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a n-layered mask film in the invention of Fornof et al. in order to improving the etching characteristics of vias and trenches as Gutsche discloses that a multilayered mask film would provide a hard mask suitable for etching of semiconductor substrates with a high aspect ratio like vias, the patterning of materials that are difficult to etch or during contact hole etching or trench etching.

Regarding claim 7, Fornof et al. discloses forming a via through the dielectric material to the underlying interconnect layer and forming a trench within the dielectric material, to a predetermined depth of the dielectric material.

Regarding claim 8, Fornof et al. discloses forming the via in the mask layer down to the first mask film 56 and forming the trench in the mask layer down to the second mask film 58.

Gutsche discloses that the mask films are patterned successively and that several patterns could be used in the layers as the layers are selectively etched with respect to the underlying layer.

Thus, it would have been within the scope of one of ordinary skill in the art at the time the invention was made to etch the trench down to the third mask film in the invention of Fornof et al. as modified by Gutsche as this would not yield any unexpected results, and as the mask layers are selectively etched it would have been

within the scope of one of ordinary skill in the art at the time the invention was made to etch the trench down to either of the fourth, third or second mask layers and still etch the trench through the dielectric layer down to a predetermined depth.

Regarding claim 9, Fornof et al. discloses forming the via through the dielectric material and forming the trench to a predetermined depth of the dielectric material.

Regarding claim 10, Fornof et al. discloses forming a via through the dielectric material, forming a trench in the mask layer down to the first mask layer and forming a trench in the dielectric material to a predetermined depth of the dielectric material.

Regarding claims 11, and 12, both Fornof et al. and Gutsche disclose that all the mask films excepting the first mask film are removed from the semiconductor device.

1. Claims 13-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fornof et al. in view of Gutsche as applied to claims 6-12 above, and further in view of Applicant's admitted prior art .

Regarding claims 13 and 15, Fornof et al. discloses forming a dielectric layer 52.

Fornof et al. discloses the claimed invention with the exception of utilizing a multi-layered dielectric layer comprising a via dielectric layer, a trench dielectric layer formed over the via dielectric layer, and an etch stop layer disposed between the trench dielectric layer and the via dielectric layer, and a barrier layer being disposed between the via dielectric layer and the interconnect layer.

Applicant's admitted prior art discloses in figs. 1 and 2, a conventional method of forming an interconnect structure of a semiconductor device, the interconnect structure

having a dielectric material deposited over an underlying interconnect layer and having a via extending through the dielectric material for establishing a connection between an underlying conductor and a trench in an upper portion of the dielectric material, wherein the dielectric material includes a via dielectric layer 12 formed over the interconnect layer 11, a barrier layer 14 disposed between the via dielectric layer 12 and the interconnect layer 11, a trench dielectric layer 13 formed over the via dielectric layer 12, and an etch stop layer 15 disposed between the trench dielectric layer 13 and the via dielectric layer 12. Where the multilayer dielectric arrangement and the barrier layer between dielectric layers are used for the purpose of preventing diffusion or migration of impurities (i.e. conductive layer material atoms) into the dielectric layers that could affect the resistance of the dielectric layer or short the circuit, and to enhance the forming of the via and the trench by etching the two dielectric layers instead of a single dielectric layer comprising both structures.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a barrier layer between the via dielectric layer and the interconnect layer and to use a multilayer dielectric layer in the invention of Fornof et al. as the Applicant's admitted prior art teaches that any one of ordinary skill in the art would use such a layer in order to prevent diffusion or migration of impurities (i.e. conductive layer material atoms) into the dielectric layers that could affect the resistance of the dielectric layer or short the circuit and to improve the formation of the dual damascene structure.

Regarding claim 14, Fornof et al. discloses that the etch stop layer may be formed of material including TEOS, among others, while Gutsche discloses that among the materials that can be used for the alternating mask films, oxides of silicon are included, Fornof et al. as modified by Gutsche discloses that as an underlying layer is patterned the uppermost mask film is removed, thus when etching through the etch stop layer, the exposed fourth mask layer could be made of the same material as the etch stop layer and removed by the same etchant as the etch stop layer, thus simultaneously forming the via through the etch stop layer and etching the fourth mask film from the semiconductor device would be accomplished, and this would have been within the scope of one of ordinary skill in the art at the time the invention was made.

Regarding claims 16 and 17, Fornof et al. discloses that the second mask film is removed as the via is formed through the barrier layer, thus it would have been within the scope of one of ordinary skill in the art at the time the invention was made that the uppermost layer would be removed when etching through the barrier layer or the etch stop layer as Fornof et al. discloses the removal of the topmost mask layer simultaneously with the removal of the barrier layer.

6. Claims 18 to 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fornof et al. in view of Gutsche et al. and Applicant's admitted prior art.

Regarding claim 18, Fornof et al. discloses a method of forming an interconnect structure using a mask layer deposited over a dielectric material which has been deposited over an underlying interconnect layer 50, comprising the steps of forming a

dielectric layer over the underlying interconnect layer 50; forming a first mask film 56 over the dielectric material 52 having a known set of properties; forming a second mask film 58 over the first mask film 56 having a known set of etch properties different from the etch properties of the first mask film, and selectively etching the mask films in multiple steps to form the interconnect structure; etching the masking films to a first predetermined depth of the mask layer without exposing the underlying dielectric and to form a via within the mask layer, and then etching the mask films to a second predetermined depth of the mask layer which is less than the first predetermined depth previously etched in the mask layer to form a trench within the mask layer.

Thus, Fornof et al. discloses the claimed invention with the exception of forming a multilayer dielectric structure comprising a via dielectric layer and a trench dielectric layer; forming a third mask film over the second mask film having etch properties substantially identical to the etch properties of the first film, and forming a fourth mask film over the third mask film having etch properties substantially identical to the etch properties of the second mask film.

Gutsche discloses a method for fabricating a hard mask on a semiconductor substrate to be applied during contact hole etching or during deep trench etching (¶[0027]) that includes forming a first mask film over the substrate having a known set of etch properties; forming a second mask film over the first mask film having a known set of etch properties different from the etch properties of the first mask film (¶[0022]); forming a third mask film over the second mask film having etch properties

substantially identical to the etch properties of the first film(¶[0022], [0024]), and forming n mask films over the third mask film having etch properties alternating according to the first and second mask films, for the disclosed intended purpose of providing a hard mask for etching of semiconductor substrates with a high aspect ratio like vias, the patterning of materials that are difficult to etch or during contact hole etching or trench etching.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a n-layered mask film in the invention of Fornof et al. in order to improving the etching characteristics of vias and trenches as Gutsche discloses that a multilayered mask film would provide a hard mask suitable for etching of semiconductor substrates with a high aspect ratio like vias, the patterning of materials that are difficult to etch or during contact hole etching or trench etching.

Applicant's admitted prior art discloses in figs. 1 and 2, a conventional method of forming an interconnect structure of a semiconductor device, the interconnect structure having a dielectric material deposited over an underlying interconnect layer and having a via extending through the dielectric material for establishing a connection between an underlying conductor and a trench in an upper portion of the dielectric material, wherein the dielectric material includes a via dielectric layer 12 formed over the interconnect layer 11, a barrier layer 14 disposed between the via dielectric layer 12 and the interconnect layer 11, a trench dielectric layer 13 formed over the via dielectric layer 12, and an etch stop layer 15 disposed between the trench dielectric layer 13 and the via

dielectric layer 12. Where the multilayer dielectric arrangement and the barrier layer between dielectric layers are used for the purpose of preventing diffusion or migration of impurities (i.e. conductive layer material atoms) into the dielectric layers that could affect the resistance of the dielectric layer or short the circuit, and to enhance the forming of the via and the trench by etching the two dielectric layers instead of a single dielectric layer comprising both structures.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use a barrier layer between the via dielectric layer and the interconnect layer and to use a multilayer dielectric layer in the invention of Fornof et al. as the Applicant's admitted prior art teaches that any one of ordinary skill in the art would use such a layer in order to prevent diffusion or migration of impurities (i.e. conductive layer material atoms) into the dielectric layers that could affect the resistance of the dielectric layer or short the circuit and to improve the formation of the dual damascene structure.

Regarding claim 19, Fornof et al. discloses forming a via in the mask layer down to the first mask film and forming a trench in the mask layer down to the second mask film, and the trench overlapping the via.

Fornof et al. as modified by Gutsche, would have a n-layered mask having n-mask films, and forming the via and the trench down to a n-mask film or n-1 mask film would have been obvious to one of ordinary skill in the art and would not provide any unexpected results.

Regarding claim 20, Fornof et al. as modified by Applicant's admitted prior art discloses forming a via through the dielectric layer and the barrier layer corresponding to the dimensions of the via formed in the mask layer, forming a trench through the trench dielectric layer corresponding to the dimensions of the trench formed in the mask layer, and the trench in the trench dielectric overlapping the via in the via dielectric layer.

Regarding claims 21 and 22, Fornof et al. teaches the removal of the mask films with the exception of the first mask film, thus it would have been obvious to one of ordinary skill in the art at the time the invention was made that the second, third and fourth mask films are removed in the process.

Response to Arguments

2. Applicant's arguments with respect to claims 1-22 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and

any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ginette Peralta whose telephone number is (703)305-7722. The examiner can normally be reached on Monday to Friday 8:00 AM- 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703)308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7722 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

GP
May 20, 2003

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800